ATTACHMENT

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a semiconductor device, a microcomputer, and electronic equipment.
[0002]
Background Art and Problem(s) to be Solved by the Invention] Generally, a setup of the timer value in timer control is performed, when [which detected the time-out of a timer by interruption etc.] it interrupts and a routine sets the value of a new timer to a timer.
[0003] However, if software like an interruption routine is made to intervene, after a time-out will occur before finishing setting the following timing value to a timer, a number cycle is required at least.
[0004] For this reason, in the timer output which needs real-time control, how real time nature is secured poses a problem.
[0005] The register which can hold the following timer value here is prepared, and the technique of setting to a timer the value held at the register concerned is also considered. According to this technique, about the real time nature of only 1 level, can be and extent reservation can be carried out.
[0006] However, on the occasion of a setup of the timer value to the register which can hold the following timer value, mediation of the interruption routine which is already beam software is needed. For this reason, by the time the time-out occurred, the software which can set up the timer value to a register in the first half was needed, and for software, it had become a big burden.
[0007] This invention is made in view of the above troubles, and the place made into the purpose aims at offer of the semiconductor device equipped with the timer function in which advanced real time nature is realizable, a microcomputer, and electronic equipment.
[0008]
[Means for Solving the Problem] This invention is a semiconductor device and is characterized by including the timer circuit which performs count actuation based on the timer value stored in the timer value setting register, and the timer control circuit which performs timer value setting control which reads a timer value from a timer information table, and is set as a timer value setting register.
[0009] Including a timer counter, when an underflow is carried out, overflow or the case where the value of a timer value setting register is set as a timer counter is sufficient as a timer counter apart from [said timer circuit] a timer value setting register, to perform count actuation based on the timer value stored in the timer value setting register, for example.
[0010] Timer value setting control is control for transmitting or loading the timer value stored for example, in the timer information table to a timer value register.
[0011] An access mediation circuit required in order to read a timer value from a timer information table may be given to timer control at dedication, and may use BASURI QUEST / bus acknowledgement function to CPU.
[0012] The timing which reads a timer value from a timer information table, and is set as a timer value setting register is good also considering for example, a timer underflow or timer overflow as a trigger.

[0013] The timer information table is memorized on the internal memory of the semiconductor device of this invention, or external memory, and includes two or more timer values continuously set as a timer value setting register at least.
[0014] The semiconductor device of this invention has the timer control circuit which reads a timer value from a timer information table, and is set as a timer value setting register. Therefore, the following timer value can be set as real time by making timer overflow and a timer underflow into a trigger at a timer value setting register.
[0015] Since a setup of a timer value can be performed according to this invention, without minding software, such as an interruption routine, the semiconductor device equipped with the timer function in which true real time is realizable can be offered.
[0016] Moreover, said timer circuit is characterized by choosing the clock source based on the clock information on said timer information table, and performing count actuation including clock information for the semiconductor device of this invention to choose the clock source which uses said timer information table in case a timer circuit performs count actuation.
[0017] By giving clock information to a timer information table, the clock source with which plurality differs according to the contents to count can be used properly. For this reason, according to this invention, the semiconductor device which equipped real time with the timer function in which a precise timer setup is possible can be offered.
[0018] Moreover, as for said timer information table, the semiconductor device of this invention is characterized by performing timer value setting control from the 2nd timer information table specified by the table [degree] pointer information of the 1st timer information table, when said timer control circuit ends the timer value setting control from the 1st timer information table including table [degree] pointer information.
[0019] According to this invention, the 1st timer information table and the 2nd timer information table can be made to link with a table [degree] pointer.
[0020] It becomes realizable [complicated timer actuation] by performing timer actuation using two or more timer information tables on which it follows, for example, various timer information, such as clock information, differs.
[0021] For this reason, according to this invention, the semiconductor device which equipped real time with the timer function in which a complicated timer setup is possible can be offered.
[0022] Moreover, as for said timer information table, the semiconductor device of this invention is characterized by performing timer value setting control from the timer information table concerned until said timer control circuit reaches said number of effective counted value including the number information of effective counted value.
[0023] Moreover, in table enabling, the semiconductor device of this invention is characterized by setting a timer value as a timer value setting register by activation of a given interruption routine, when said timer control circuit performs timer value setting control from a timer information table and is not table enabling.
[0024] In here, the program for for example, timer control may be made to perform a setup of table enabling state.
[0025] According to this invention, the semiconductor device equipped with the timer function in which count actuation can also be performed based on the timer value read from the timer information table, and count actuation can also be performed based on the timer value set as the timer value setting register by activation of a predetermined interruption routine can be offered by changing table enabling and a table disable if needed.
[0026] Moreover, the semiconductor device of this invention is a microcomputer which contains the semiconductor device of a publication in one of the above, and is characterized by including a timer information table generation means by which said semiconductor device generates said timer information table on accessible memory.
[0027] As for a timer information table, it is desirable to generate, by the time a timer circuit becomes to timer enable.

[0028] The microcomputer of this invention can set in hard the timer value memorized by the timer information table on memory as a timer circuit, without minding the interruption routine by software. Therefore, according to this invention, the microcomputer which equipped real time with the timer function which can set up a timer value can be offered.
[0029] In addition, you may make it said timer information table generation means generate a timer information table on memory with said accessible semiconductor device based on the information for generating said timer information table including the storage means which memorized the information for generating said timer information table.
[0030] The data used as the processing object of the program which generates for example, a timer information table are sufficient as the information for generating said timer information table, and the program itself is sufficient as it.
[0031] Moreover, the microcomputer of this invention is characterized by said timer information table generation means generating a timer information table for every range countable [with the same clock source].
[0032] In case for example, count actuation is performed with the range countable [with the same clock source] in here, the range where the frequency used as criteria is the same is said.
[0033] The microcomputer of this invention is characterized by said timer information table generation means generating said timer information based on feedback information.
[0034] According to this invention, the microcomputer equipped with the timer function which can be set as real time for the timer value in which feedback information was reflected can be offered.
[0035] The electronic equipment of this invention is characterized by including the entry-of-data means used as the microcomputer of a publication, and the processing object of said microcomputer, and the output means for outputting the data processed with said microcomputer in one of the above.
[0036] According to the electronic equipment of this invention, electronic equipment equipped with the timer function in which true real time nature is required can be offered.
[0037]
[Embodiment of the Invention] 1. Explain the suitable operation gestalt of this invention to a detail using a drawing below a semiconductor device.
[0038] Drawing 1 is an example of the block diagram of the semiconductor device of the gestalt of this operation, and is the case where it has a memory access mediation circuit in a timer control circuit. In addition, in this drawing, the semiconductor device 10 of this operation gestalt can be used as the component of arbitration about the other block that what is necessary is just to include the timer circuit 20, the timer control circuit 30, and memory 50 at least.
[0039] The timer circuit 20 contains the timer value setting register 22, a timer counter 24, and the interruption control circuit 26. A timer counter 24 outputs the timer overflow signal 28, when count-up actuation is performed and counted value turns to zero.
[0040] In addition, a down counter is sufficient as the timer circuit 20, and when a counter value becomes zero in this case, it outputs a timer underflow signal. Although explained taking the case of the case where the timer circuit 20 is [following] a rise counter, when it is a down counter, it can control similarly (when using a timer underflow signal).
[0041] Moreover, the interruption control circuit 26 will turn and output the timer overflow signal 28 concerned to the timer control circuit 30, if the timer overflow signal 28 is received.
[0042] The timer control circuit 30 is constituted so that timer control may be performed based on the timer information table 52, and it includes the memory access mediation circuit 32.
[0043] The timer control circuit 30 will perform processing which reads a timer value from the timer information table 52, and is transmitted to a timer set point register, if the timer overflow signal 28 is received.
[0044] The memory access mediation circuit 32 performs processing which reads the contents of the timer information table 52 established on memory 50 to predetermined timing after performing mediation with the memory access from CPU.
[0045] CPU40 performs system-wide control, directions of the instruction to each block in a system, or

executive operation of various applications.
[0046] Memory 50 consists of RAM etc. and the timer information table 52 is memorized. In addition, in having the timer information table 52 on RAM, by the time it performs timer control, you may make it an application program etc. generate. Moreover, you may make it make the timer information table 52 memorize beforehand on ROM.
[0047] The port output control circuit 60 is a circuit which generates a port output required for various control etc. based on timer overflow.
[0048] In addition, although the configuration of an about was explained by drawing 1 when it had the memory access mediation circuit 32 in the timer control circuit 30, you may make it use the bus mediation function of CPU for mediation of memory access.
[0049] Drawing 2 is other examples of the block diagram of the semiconductor device of the gestalt of this operation, and is the cases where the bus mediation function of CPU is used for mediation of memory access. In addition, in this drawing, the semiconductor device 110 of this operation gestalt can be used as the component of arbitration about the other block that what is necessary is just to include the timer circuit 120, the timer control circuit 130, and memory 150 at least.
[0050] It is the configuration same about the timer circuit 120, CPU140, memory 150, and the port output control circuit 160 as the timer circuit 20 of drawing 1 , CPU40, memory 50, and the port output control circuit 60.
[0051] Since the timer control circuit 130 of the gestalt of this operation here does not have the memory access mediation circuit like drawing 1 , access ****** differs from the timer control circuit of drawing 1 to the timer information table 152 on memory 150 using the bus mediation function of CPU. That is, the timer control circuit 130 will output the BASURI QUEST signal 132 to CPU, if access is needed to a timer information table.
[0052] And a memory access demand is advanced for the bus acknowledgement signal 134 from CPU after ********, and the access data on the CPU bus 154 are received after fixed time amount.
[0053] Drawing 3 is drawing for explaining the configuration of the timer control circuit of the gestalt of this operation.
[0054] The timer control circuit 400 includes the timer control state machine 410, AddrPointer420, BaseRegister430 and TempCNT440, and the memory access demand circuit 450.
[0055] The timer control state machine 410 is a state machine which controls the control and memory access to a timer circuit.
[0056] AddrPointer420 is an internal address pointer for memory access. The start address of the timer value of a timer information table is stored in the beginning of processing of a given timer information table. The start address of a timer value applies a predetermined offset value to the value of BaseRegister430, and is called for.
[0057] BaseRegister430 stores the start address of a timer information table. Before starting a timer, the value of the start address of the timer information table used as the candidate for access is stored in BaseRegister430 by the software which performs timer control. When two or more timer information tables are accessed continuously, after timer value transfer processing of the timer information table concerned is completed, the table [degree] pointer of the timer information table concerned is stored in BaseRegister430.
[0058] TempCNT440 is an internal counter circuit for counting the number of the timer values which read from the timer information table and were transmitted to the timer circuit, and judging termination of a transfer of the timer value from the timer information table concerned.
[0059] The memory access demand circuit 450 performs processing which requires a required value of memory from the table on memory using AddrPointer420 in response to the demand from the timer control state machine 410.
[0060] In addition, in the timer control circuit of drawing 1 , the memory access demand circuit 450 will perform an access request to the memory access mediation circuit 32 (refer to drawing 1), and a memory access demand circuit will perform a bus access demand to CPU140 (refer to drawing 2) in the timer control circuit of drawing 2 .

[0061] Drawing 4 is drawing for explaining the timer information table generated by memory.
[0062] Here, taking the case of the case where three timer information tables, the timer information table A, the timer information table B, and the timer information table C, are generated, it explains on memory.
[0063] The information which shows the existence of the timer information table which should be linked to a degree is stored in LinkEnable 210, 1310, and 1410 here. If it is "1" like and will finish transmitting all the timer values of the timer information table concerned to 210 or 220, processing will be moved to the following timer information table shown in a link address. Moreover, processing will be ended, if it is "0" and will finish transmitting all the timer values of the timer information table concerned.
[0064] The start address of a timer information table which should move control next is stored in link addresses 220, 1320, and 1420. For example, when moving control in order of the timer information table A, the timer information table B, and the timer information table C, the start address of the timer information table B is stored in 220, and the start address of the timer information table C is stored in 1320. Since there is no timer information table which moves control next when LinkEnable is 0 like 1420, this value is not referred to.
[0065] The count of a transfer of the timer value stored in this timer information table is stored in 230, 1330, and 1430 transfer timer values. For example, when 20 is set to the number of transfer timer values like 230, the 20 timer values from 270-0 to 270-19 are transmitted to a timer circuit.
[0066] The information for specifying the clock source of a timer is stored in the clock sources 240, 1340, and 1440. It consists of gestalten of this operation so that the clock source used for count actuation can be chosen from the clock source with which two or more frequencies differ. For example, to the timer value transmitted from the timer information table A, count actuation is performed using the 1MHz clock source, count actuation is performed using the 500kHz clock source to the timer value transmitted from the timer information table B, and count actuation is performed using the 250kHz clock source to the timer value transmitted from the timer information table C.
[0067] Thus, with the gestalt of operation, a timer information table is generated for every range in which the same clock source count is possible.
[0068] In case for example, count actuation is performed, the range where the frequency used as criteria is the same is called range countable [with the same clock source].
[0069] The transfer data length at the time of transmitting a timer value to a timer is stored in the data sizes 250, 1350, and 1450. For example, when transmitting per cutting tool, "0" may be set, and when transmitting to a word unit, you may make it set "1." In addition, it is unnecessary when always transmitting by the fixed length.
[0070] IRQEN 260, 1360, and 1460 stores the information about whether the termination is notified to CPU through interruption (IRQ), when a transfer of all the timer values in the table concerned is completed. For example, it is good also as those with a notice by IRQ at the notice nothing by IRQ, and the time of "1" at the time of "0."
[0071] The timer value 270-0 to 270-19, 1370-0 to 1370-9, and the timer value with which 1470-0 to 1470-11 is transmitted to a timer value setting register are stored.
[0072] In addition, about the component of a timer information table, only a timer value is indispensable, and it is arbitrary about other components. moreover, the class of component -- it constructs and doubling is not restricted to the example of drawing 4 , either.
[0073] Moreover, drawing 5 is drawing for explaining the relation between a timer information table and a timer output.
[0074] Section A, Section B, and Section C are the sections when the timer main force is controlled by the timer information tables A, B, and C, respectively.
[0075] In this example, 1MHz, 500kHz, and 250kHz are used for the clock source in the case of performing timer control of each sections A, B, and C, respectively. Thus, with the gestalt of this operation, a timer information table is generated for every range countable [with the same clock source].
[0076] In Section A, the timer value 270-0 to 270-19 of the timer information table A of drawing 4 is

followed, and they are the small sections A0, A1, and A2 within Section A. -- A timer output is performed. That is, whenever each counted value overflows, the change of (311,312,313 --), H of a port output, and L is performed.
[0077] The same is said of Sections B and C. Thus, with the gestalt of this operation, a timer output is performed based on the timer value stored in each timer information tables A, B, and C (311,312,313 --), and the port output 360 as shown in 360 based on a timer output is generated.
[0078] In addition, since interruption can be generated to the timing of 390 by what is set to IRQEN=1 on Table C, termination of the timer control on a timer information table can be checked by the interruption concerned.
[0079] Moreover, by giving a toggle function to a port output circuit (60 of drawing 1 , 160 reference of drawing 2), for example, it is possible to apply the port output 360 shown in drawing 5 as a PWM-Pulse Width Modulation output.
[0080] Drawing 6 is a flow chart Fig. for explaining the example of control performed by the timer state machine.
[0081] If it becomes table timer enabling, the access address of the beginning of a timer value is calculated from BaseRegister and timer value storing offset, and this is stored in AddrPointer (steps S10 and S20). Timer value storing offset is calculated here according to the difference of the start address of a table, and the start address of the first timer value used as a processing object. Moreover, the value of BaseRegister will be stored by predetermined application software, by the time the timer conte rule on a timer information table starts.
[0082] Next, the number of transfer timer values is loaded from the timer information table on memory, and it stores in a TempCNT register (step S30).
[0083] And processing to steps S50-S90 is repeated until TempCNT is set to 0.
[0084] Based on the address which AddrPointer puts first, a timer value is loaded from the timer information table on memory (step S50).
[0085] And the loaded timer value is transmitted to the timer value setting register of a timer circuit (step S60).
[0086] And the decrement of the TempCNT is carried out, and it updates so that AddrPointer may point out the address of the following timer value (steps S70 and S80).
[0087] And if timer overflow is detected, it will return to step S40 again (step S90).
[0088] Moreover, if TempCNT is set to 0, processing to steps S100-S130 will be performed.
[0089] If it is IRQEN=1 first, it will start by interrupting (steps S100 and S110).
[0090] And it updates so that the value of AddrPointer may point out the head of the timer value of the following timer information table in the case of LinkEnable=1, and in not being LinkEnable=1, it ends processing (step S130).
[0091] Next, generation of a timer information table is explained.
[0092] Drawing 7 is a processing flow at the time of an application program generating a timer information table on memory.
[0093] Probably, it judges in required no, and the control on a timer information table does not generate a timer information table, in being unnecessary (step S210). In addition, when not generating a timer information table, timer control by the usual software interrupt which does not mind a timer control circuit can also be performed.
[0094] In performing control on a timer information table, either ** - ** are processed and it generates a timer information table (step S220).
[0095] ** Develop the timer value which should be set up using a predetermined formula on a timer information table.
[0096] ** Develop the value used as the base of the timer beforehand stored in ROM on the timer information table on RAM.
[0097] ** Perform the operation by predetermined operation expression to the value used as the base of the timer beforehand stored in ROM, calculate a timer value, and develop on the timer information table on RAM.

[0098] When generation of the following timer information table is needed here, the head pointer of degree table is set to the link address of the table concerned, and in order to generate the following timer information table, it goes to step S220 (step S240).
[0099] When the following timer information table is not required, timer information table generation processing is ended here, and the address of the timer information table first used for BaseRegister of a timer control circuit is set up (step S250).
[0100] And a table timer is enabled (step S260).
[0101] If a table timer is enabling, a timer control circuit will perform a timer conte rule (refer to drawing 4).
[0102] 2. Microcomputer drawing 8 is an example of the hardware block diagram of the microcomputer of the gestalt of this operation.
[0103] This microcomputer 700 contains CPU510, cache memory 520, the LCD controller 530, a reset circuit 540, the timer circuit 550, a real time clock (RTC) 560, DAM570, the interruption controller 580, serial interface 590, a bus controller 600, A/D converter 610, D/A converter 620, input port 630, an output port 640, I/O Port 650, clock generation equipment 560, a prescaler 570 and the various bus 680 grades that connect them, and various pin 690 grades.
[0104] The timer circuit 550 contains the timer circuit 20 and timer control circuit 30 grade which were explained by drawing 1 .
[0105] A timer information table is generated by RAM720.
[0106] The microcomputer of the gestalt of this operation can set in hard the timer value memorized by the timer information table on RAM as a timer circuit, without minding the interruption routine by software. For this reason, the microcomputer equipped with the timer function in which advanced real time nature is realizable can be offered.
[0107] 3. An example of the block diagram of the electronic equipment of the gestalt of this operation is shown in electronic equipment drawing 9 . This electronic equipment 800 contains a microcomputer (or ASIC) 810, the input section 820, memory 830, the power-source generation section 840, LCD850, and the sound output section 860.
[0108] Here, the input section 820 is for inputting various data. A microcomputer 810 will perform various processings based on the data inputted by this input section 820. Memory 830 serves as working areas, such as a microcomputer 810. The power-source generation section 840 is for generating the various power sources used by electronic equipment 800. LCD850 is for outputting various kinds of images (an alphabetic character, an icon, graphic, etc.) which electronic equipment displays. The sound output section 860 is for outputting various kinds of sounds (voice, game sound, etc.) which electronic equipment 800 outputs, and can realize the function by hardware, such as a loudspeaker.
[0109] The electronic equipment of the gestalt of this operation is for example, an PWM timer, a printer, a pocket device, a toy, etc. It is effective when performing the sound output by the motor control and the PWM output using especially an PWM timer, the infrared remote control output by the PWM output, etc.
[0110] According to the electronic equipment of the gestalt of this operation, electronic equipment equipped with the timer function in which true real time nature is required can be offered.
[0111] In addition, this invention is not limited to this operation gestalt, but deformation implementation various by within the limits of the summary of this invention is possible for it.
[0112] For example, the contents of the timer information table are not restricted to the example explained by drawing 4 .
[0113] Moreover, with the gestalt of this operation, although the difference in the clock source explained taking the case of the case where a table is divided, it is not restricted to this. For example, in having the table format which can be judged on the timer information table of 1, even if the clock sources differ change of the clock source, it is not necessary to prepare two or more tables.
[0114] Moreover, a table may be divided by change of the transfer data size at the time of transmitting other control information but, for example, a timer value, that the clock source is the same.
[0115] moreover, conte rule information may be the same as the clock source, transfer data size, etc., or

a table may be divided with user-friendliness. Namely, 5 which covered the all when the control with which there are timer information tables A, B, A, C, and D which serve as a basic pattern, for example, and these were combined in order of arbitration occurred! The case where do not create the table information on a passage beforehand, but construct on real time and it controls on it is sufficient. In this case, even before a transfer of the timer value of the last of the table under current reference is completed, it is necessary to rewrite the link address to the following table.

[Translation done.]